AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions, and listings, of claims:

1. (Original) A method of controlling access to a shared memory of a multiprocessor system, the multiprocessor system comprising a first bus and a second bus coupled to the shared memory, the first bus coupled to a first processor, and the second bus coupled to a second processor, the method comprising the steps of:

requesting exclusive access to a first memory location of the shared memory by the first processor;

granting exclusive access to the first memory location of the shared memory to the first processor; and

A1

allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location.

2. (Original) The method of claim 1, the step of requesting exclusive access comprising the steps of:

asserting a lock signal on the first bus; and

sending a lock request from the first processor to a memory controller coupled to the first bus, the second bus, and the shared memory.

3. (Original) The method of claim 2, the step of asserting a lock signal further comprising the step of:

asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains two memory address data.

4. (Original) The method of claim 2, the step of requesting exclusive access further comprising the step of:

forwarding the lock request from the memory controller to a switch; and

signaling the first processor to retry the lock request.

5. (Original) The method of claim 4, the step of granting exclusive access comprising the steps of:

signaling the memory controller by the switch to retry the lock request;

assigning exclusive access to the first memory location by the switch;

notifying the memory controller of the exclusive access assigned in the assigning step; and

granting exclusive access to the first memory location by the memory controller responsive to a retry of the lock request by the first processor.

6. (Original) The method of claim 5, the step of assigning exclusive access to the memory location by the switch comprising the steps of:

A1

determining if the first memory location is currently assigned;

saving a lock request information if the first memory locations is not currently assigned; and

sending the lock request information to the memory controller.

7. (Original) The method of claim 6, the lock request information comprising:

a node ID of the first processor;

a cycle ID of the first processor; and

memory address data for a first memory location.

8. (Original) The method of claim 7, the memory address data comprising:

a first memory address; and

a second memory address,

wherein the first memory address can be non-contiguous with the second memory address.

9. (Original) The method of claim 1, further comprising the step of:

releasing exclusive access to the first memory location.

10. (Original) A method of controlling access to memory of a multinodal computer system, the multinodal computer system comprising a plurality of multiprocessor nodes, the method comprising the steps of:

requesting exclusive access to a first memory location of a shared memory by a first processor of a first multiprocessor node the plurality of multiprocessor nodes;

granting exclusive access to the first memory location of the shared memory to the first processor; and

allowing access to a second memory location of the shared memory to a second processor of a second multiprocessor node of the plurality of multiprocessor nodes while the first processor has exclusive access to the first memory location.

A1

11. (Original) The method of claim 10, the requesting step comprising:

asserting a lock signal on a first bus, the first bus coupling the first processor and a first memory controller of the first multiprocessor node; and

sending a lock request to the first memory controller;

forwarding the lock request from the first memory controller to a switch, the switch coupled to each of the plurality of multiprocessor nodes.

12. (Currently Amended) The method of claim 10, the shared memory comprising:

a first memory coupled to the first memory controller; and

a second memory coupled to a second memory controller of a different multiprocessor node of the plurality of multiprocessor nodes;.

13. (Original) The method of claim 12, the step of asserting a lock signal comprising the step of:

asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains a first memory address data and a second memory address data.

14. (Original) The method of claim 13, the first memory address data referencing the first memory and the second memory address data referencing the second memory.

15. (Original) The method of claim 13, the first memory address data referencing the second memory and the second memory address data referencing the first memory.

16. (Currently Amended) The method of claim 10, the step of requesting exclusive access further comprising ~~the step of~~:

forwarding the lock request form the first memory controller to the switch; and

signaling the first processor to retry the lock request.

17. (Original) The method of claim 10, the step of granting exclusive access comprising the steps of:

signaling the first memory controller to retry the lock request;

assigning exclusive access to the memory location by the switch;

notifying the memory controller of the exclusive access assigned in the assigning step; and

assigning exclusive access to the first memory location by the first memory controller responsive to a retry of the lock request by the first processor.

18. (Original) The method of claim 17, the step of assigning exclusive access to the memory location by the switch comprising the steps of:

determining if the first memory location is currently assigned;

saving a lock request information if the first memory location is not current assigned; and

broadcasting the lock request information to each memory controller of each of the plurality of multiprocessor nodes.

19. (Original) The method of claim 18, the lock request information comprising:

a node ID of the first multiprocessor node;

a cycle ID of the first processor; and

a memory address data for the first memory location.

20. (Original) The method of claim 10, further comprising the step of:

releasing exclusive access to the first memory location.

21. (Currently Amended) A computer system for utilizing a shared memory, the computer system comprising:

a first multiprocessor node, comprising:

a first process bus;

a first processor, coupled to the first processor bus, the first processor comprising:

circuitry to generate an exclusive access request for a first memory location ~~to the first memory controller~~;

a second processor bus;

a second processor, coupled to the second processor bus, the second processor adapted to ~~perform the step of~~:

~~requesting~~ request access to a second memory location;

a first memory;

a first memory controller, coupled to the first processor bus, the second processor bus, and the first memory, the first memory controller adapted to ~~perform the steps of~~:

~~allowing~~ allow exclusive access to the first memory location by the first processor; and

~~allowing~~ allow access to the second memory location by the second processor while the first processor has exclusive access to the first memory location.

22. (Currently Amended) The computer system of claim 21, further comprising:

a second multiprocessor node, comprising:

a third process bus;

a third processor, coupled to the third processor bus, the third processor adapted to ~~perform the executable step of~~:

~~requesting~~ request access to a third memory location;

a second memory;

a second memory controller, coupled to the third processor bus, and the first memory, the second memory controller adapted to ~~perform the steps of~~:

~~allowing~~ allow exclusive access to the first memory location by the first processor;

~~allowing~~ allow access to the second memory location by the second processor while the first processor has exclusive access to the first memory location; and

~~allowing~~ allow access to the third memory location by the third processor while the first processor has exclusive access to the first memory location; and

a switch, coupled to the first memory controller and the second memory controller, for switching transactions between the first multiprocessor node and the second multiprocessor node.

23. (Original) The computer system of claim 22, the first memory location comprising:

a first portion in the first memory; and

a second portion in the second memory.

24. (Original) The computer system of claim 22,

wherein the first memory location is in the first memory, and

wherein the second memory location is in the first memory.

25. (Original) The computer system of claim 22,

wherein the first memory location is in the first memory, and

wherein the third memory location is in the first memory.

26. (Original) The computer system of claim 22,

wherein the first memory location is in the second memory, and

wherein the third memory location is in the second memory.

27. (Original) The computer system of claim 22,

wherein the first memory location is in the second memory, and

wherein the third memory location is in the first memory.

28. (Original) The computer system of claim 22, the switch comprising:
a lock register for storing a lock control information.

29. (Original) The computer system of claim 28, the lock control information comprising:
a node ID corresponding to the first processor;
a cycle ID corresponding to the first processor; and
a first memory address corresponding to the first memory location.

30. The computer system of claim 29, the lock control information further comprising:
a second memory address corresponding to the first memory location.

A1

31. (Currently Amended) The computer system of claim 29, the switch comprising:
circuitry to signal the first memory controller to retry ~~the step of~~ allowing exclusive access to the first memory location by the first processor;
circuitry to arbitrate among requests for exclusive access to the first memory location;
circuitry to broadcast the lock control information to the first memory controller and the second memory controller.

32. (Original) The computer system of claim 31, the first memory controller further comprising:
circuitry to signal the first processor to retry the exclusive access request;
circuitry to shadow the lock control information broadcast by the switch; and
the second memory controller further comprising:
circuitry to shadow the lock control information broadcast by the switch.

33. (Original) The computer system of claim 30, wherein the first memory address can be in either the first memory or the second memory, and

wherein the second memory address can be in either the first memory or the second memory.

34. (New) The method of claim 1, wherein requesting exclusive access comprises:

sending a lock request from the first processor to a first memory controller coupled to the shared memory;

forwarding the lock request from the memory controller to a switch; and

the switch broadcasting lock request information to the first memory controller and at least another memory controller.

35. (New) The method of claim 34, further comprising:

each of the first memory controller and at least another memory controller storing the lock request information.

36. (New) The method of claim 35, further comprising the switch storing the lock request information in a register in the switch,

wherein the memory controllers also store the switch request information in respective registers in the memory controllers.